



ES7154H

24-bit I²S Audio DAC with 2 Vrms Output

GENERAL DESCRIPTION

The ES7154H is a low cost 14-pin stereo digital to analog converter. The ES7154H can accept I²S serial audio data format up to 24-bit word length. The device uses advanced multi-bit Δ - Σ modulation technique to convert data into two channel analog outputs. The multi-bit Δ - Σ modulator makes the device with very low sensitivity to clock jitter and very low out of band noise.

The device integrates a charge pump to generate negative supply from 5V supply, thus providing ground centered 2 Vrms analog output.

FEATURES

- 102 dB SNR
- -85 dB THD+N
- Up to 100 kHz sampling frequency
- I²S audio data format, 16-24 bits
- Single power supply 4V to 5.25V
- Support non standard audio clocks like 25 MHz or 26 MHz

APPLICATIONS

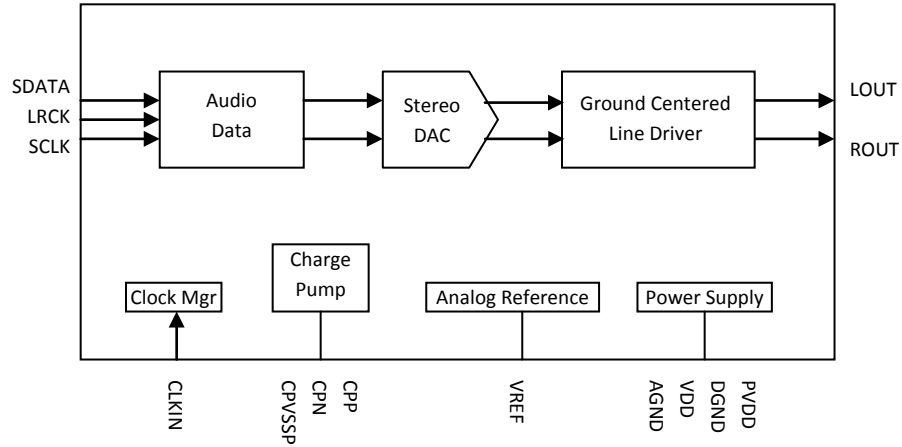
- OTT
- STB
- Digital TV
- DVD player

ORDERING INFORMATION

ES7154H -40°C ~ +85°C
SOIC-14

1.	<i>BLOCK DIAGRAM</i>	3
2.	<i>PIN OUT AND DESCRIPTION</i>	3
3.	<i>TYPICAL APPLICATION CIRCUIT</i>	4
4.	<i>CLOCK MODES AND SAMPLING FREQUENCIES</i>	4
5.	<i>DIGITAL AUDIO INTERFACE</i>	4
6.	<i>POWER UP AND DOWN</i>	5
7.	<i>ELECTRICAL CHARACTERISTICS</i>	5
	ABSOLUTE MAXIMUM RATINGS.....	5
	RECOMMENDED OPERATING CONDITIONS	5
	DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS	5
	POWER CONSUMPTION CHARACTERISTICS	6
	SERIAL AUDIO PORT SWITCHING SPECIFICATIONS	6
8.	<i>PACKAGE</i>	7
9.	<i>CORPORATE INFORMATION</i>	8

1. BLOCK DIAGRAM

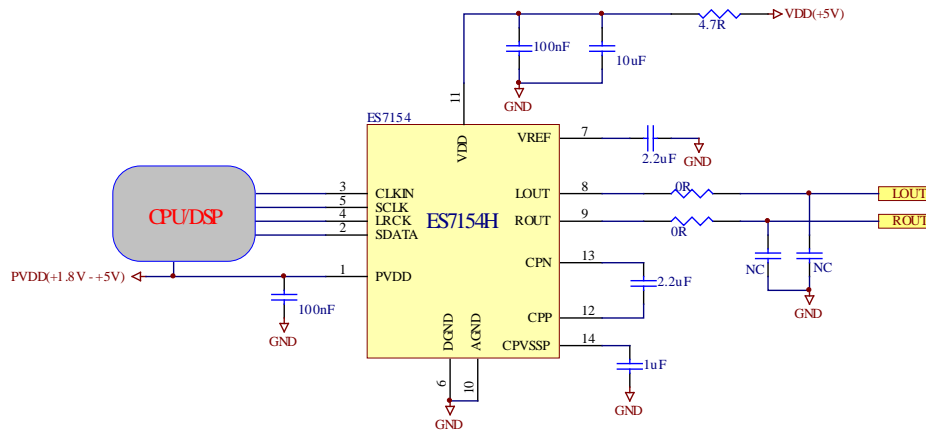


2. PIN OUT AND DESCRIPTION

PVDD	1	ES7154H	14	CPVSSP
SDATA	2		13	CPN
CLKIN	3		12	CPP
LRCK	4		11	VDD
SCLK	5		10	AGND
DGND	6		9	ROUT
VREF	7		8	LOUT

PIN	NAME	I/O	DESCRIPTION
1	PVDD	Supply	Digital IO supply
2	SDATA	I	Audio data
3	CLKIN	I	Master clock
4	LRCK	I	Audio data left and right clock
5	SCLK	I	Audio data bit clock
6	DGND	Supply	Digital ground
7	VREF		Decoupling capacitor
8	LOUT	O	Left analog output
9	ROUT	O	Right analog output
10	AGND	Supply	Analog ground
11	VDD	Supply	Power supply
12	CPP		Charge pump capacitor top
13	CPN		Charge pump capacitor bottom
14	CPVSSP		Charge pump filtering

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

According to the sampling rate, the device can work in two speed modes, single speed and double speed. Table 1 lists the typical clock modes supported by the device.

Table 1 Speed Mode and CLKIN/LRCK Ratio

MODE	Sampling Rate	CLKIN/LRCK Ratio
Single Speed	8kHz – 50kHz	32, 64, 128, 192, 256, 384, 512, 768, 1024
Double Speed	84kHz – 100kHz	128, 192, 256, 384, 512, 768, 1024

5. DIGITAL AUDIO INTERFACE

The ES7154H can accept I²S serial audio input data from 16-bit to 24-bit. The device can detect the data word length automatically. The relationship of SDATA, SCLK and LRCK for the format is illustrated through Figures 2.

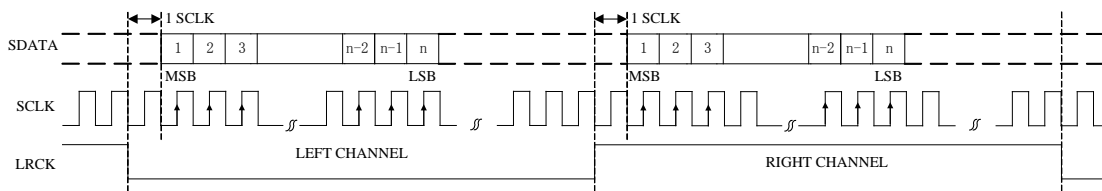


Figure 2 I²S Serial Audio Data Format Up To 24-bit

6. POWER UP AND DOWN

Upon applying VDD, the device will reset itself and enter power down state. During this state, the device clamps outputs to ground and power down the operation except for clock management unit. Once proper CLKIN and LRCK clocks are applied, the device will leave power down state and enter the normal operation.

Power down can be achieved by removal of VDD, or by first stopping LRCK and then stopping CLKIN.

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+5.5V
Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDD	4	5	5.25	V
PVDD	1.6	1.8	5.25	V

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDD=5V, PVDD=1.8V, AGND=0V, DGND=0V, ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weight)	95	102	105	dB
THD+N	-88	-85	-80	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	40			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB

Stopband Attenuation	40			dB
Analog Output				
Full Scale Output Level	1.8	2	2.1	Vrms

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
PVDD=1.8V, VDD=5V		70		mA
Power Down Mode				
DVDD=1.8V, VDD=5V		2		mA

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	-10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

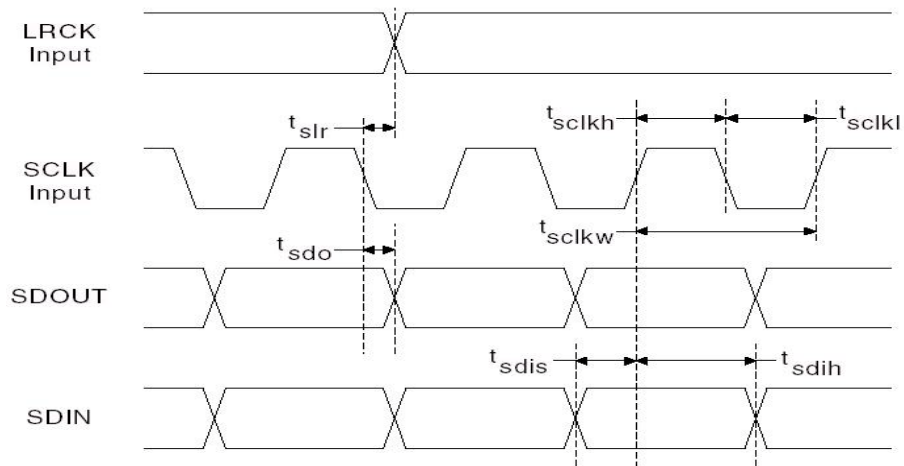
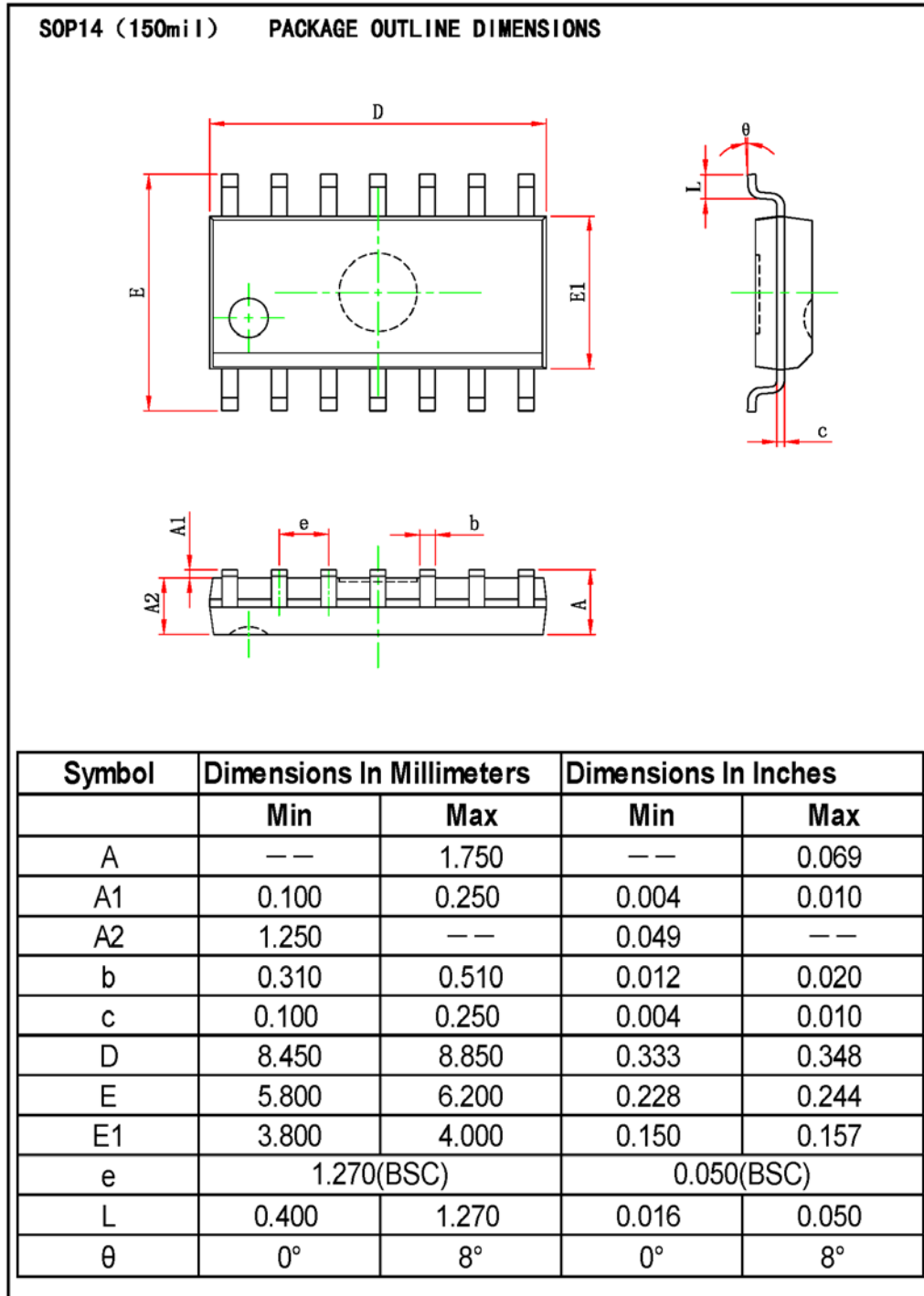


Figure 8 Serial Audio Port Timing

8. PACKAGE



9. CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

No. 1355 Jinjihu Drive, Suzhou Industrial Park, Jiangsu, P.R. China, Zip Code 215021

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: info@everest-semi.com

