110A



# **60V N-Channel MOSFET**

## (P6)

60V

## Lead Free Package and Finish

# $\overline{V}_{ m DSS}$ $R_{ m DS(ON)}(MAX)$ $I_{ m D}{}^a$

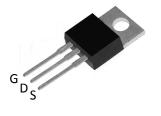
 $8m\Omega$ 

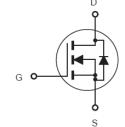
## **Applications:**

- Power Supply
- DC-DC Converters

### Features:

- Lead Free
- Low R<sub>DS(ON)</sub> to Minimize Conductive Loss
- Low Gate Charge for Fast Switching Application
- Optimized B<sub>VDSS</sub> Capability





TO-220

Package Not to Scale

# **Ordering Information**

Part Number	Package	Brand
PTP08N06N	TO-220	ľ

## **Absolute Maximum Ratings**

### Tc=25°C unless otherwise specified

Symbol	Parameter	Value	Unit
$V_{ m DSS}$	Drain-to-Source Voltage	60	V
${ m I_D}^a$	Continuous Drain Current	110	
Ідм	Pulsed Drain Current @V <sub>G</sub> =10V	439	Α
D	Power Dissipation	156	W
$P_{D}$	Derating Factor above 25°℃	1.04	W/°C
$V_{GS}$	Gate-to-Source Voltage	+/-20	V
Eas	Single Pulse Avalanche Energy (L=1mH)	800	mJ
Ias	Pulsed Avalanche Energy	Figure 9	A
T <sub>J</sub> and T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175	$^{\circ}\!\mathbb{C}$

## Thermal Resistance

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
Rөлс	Junction-to-Case			0.96	°C/W	Water cooled heatsink, P <sub>D</sub> adjusted for a peak junction Temperature of 175°C

#### Note:

a: Calculated continuous current based upon maximum allowable junction temperature +175 °C. Package limitation current is 80A.



**OFF Characteristics** T=25°C unless otherwise specified

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Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
Bvdss	Drain-to-Source Breakdown Voltage	60			V	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA
ī	IDSS Drain-to-Source Leakage Current			1	11 Δ	$V_{DS}=48V, V_{GS}=0V$
IDSS				100		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =125 °C
ī	Gate-to-Source Forward Leakage			100	A	$V_{GS}=+20V$
Igss	Gate-to-Source Reverse Leakage			100	nA	$V_{GS}$ = -20 $V$

ON Characteristics T<sub>2</sub>=25°C unless otherwise specified

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
Rds(on)	Static Drain-to-Source On-Resistanc		6.5	8	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =24A
$V_{\text{GS(TH)}}$	Gate Threshold Voltage.	2		4	V	$V_{GS}=V_{DS}$ , $I_{D}=250uA$

**Dynamic Characteristics** Essentially independent of operating temperature

Dynamic	Characteristics L	Essentially independent of operating temperature						
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions		
Ciss	Input Capacitance		3396			V -0V V -55V		
Coss	Output Capacitance		435		рF	$V_{GS}=0V, V_{DS}=55V, f=1.0MHz$		
Crss	Reverse Transfer Capacitance		151		]	I-1.0IVIIIZ		
Qg	Total Gate Charge		51					
Qgs	Gate-to-Source Charge		22		пC	$V_{DD}=30V, I_{D}=55A, V_{GS}=10V$		
Qgd	Gate-to-Drain ("Miller") Charge		15					
Td(on)	Turn-in Delay Time		14					
Tr	Rise Time		44		nS	$V_{DD}=30V, I_{D}=55A, V_{G}=10V,$		
Td(off)	Turn-off Delay Time		31		nS	$R_G=2.5\Omega$		
Tf	Fall Time		12					

Source-Drain Diode Characteristics T<sub>2</sub>=25°C unless otherwise specified

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
$V_{\mathrm{SD}}$	Diode Forward Voltage			1.2	V	$I_S=24A, V_{GS}=0V$
Trr	Reverse Recovery Time			78.5	nS	Is=38A, di/dt=100A/μs
Qrr	Reverse Recovery Charge	·		112.0	nC	15-30A, ui/ut-100A/μS



## Typical Characteristics

Figure 1. Maximum Power Dissipation V.S Case Temperature

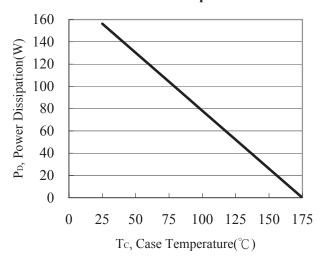


Figure 2. Maximum Continuous Drain Current V.S Case Temperature

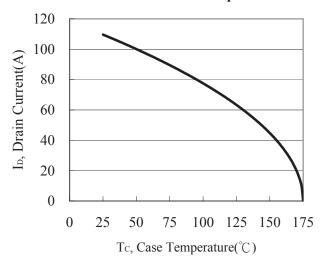


Figure 3. Typical Output Characteristics

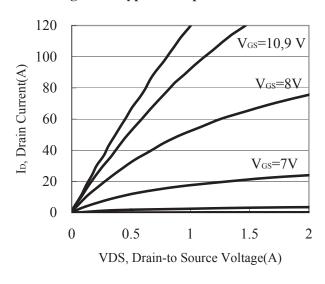


Figure 4. Breakdown Voltage V.S Junction Temperature

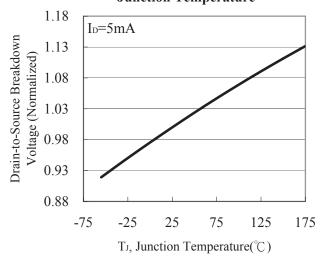


Figure 5. Threshold Voltage V.S Junction Temperature

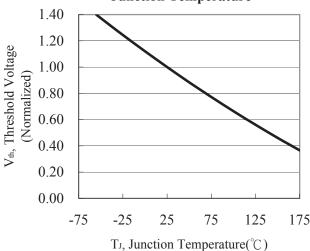
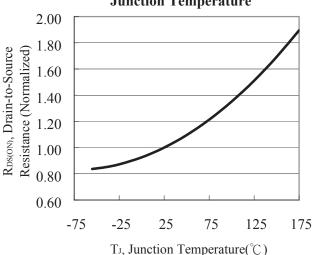


Figure 6. Drain-to-Source Resistance V.S Junction Temperature





# **Typical Characteristics**

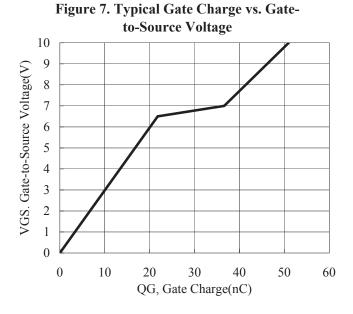


Figure 8. Typical Capacitance vs. Drainto-Source Voltage

4000

Ciss

1000

Coss

Crss

Crss

15

0

Figure 9. Unclamped Inductive Switching Capability

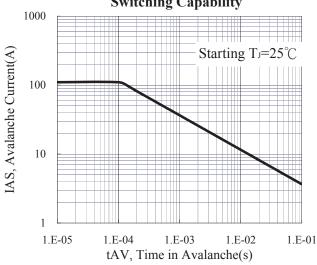


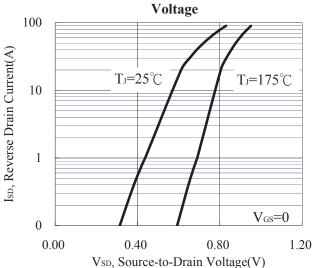
Figure 10. Source-Drain Diode Forward

30

VDS, Drain Voltage(V)

45

60





#### **TEST CIRCUITS AND WAVEFORMS**

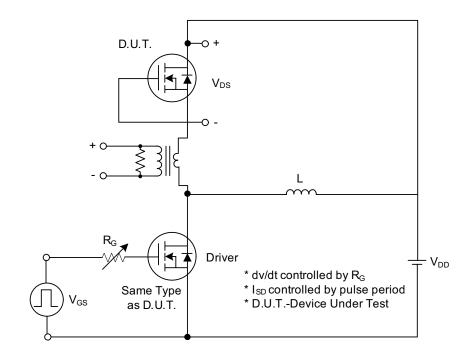


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

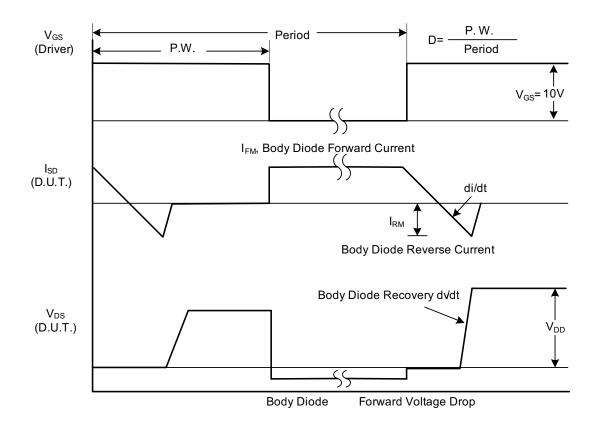


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



### TEST CIRCUITS AND WAVEFORMS (Cont.)

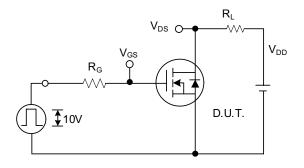


Fig. 2.1 Switching Test Circuit

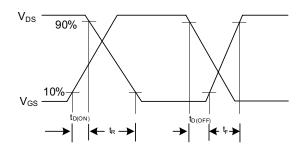


Fig. 2.2 Switching Waveforms

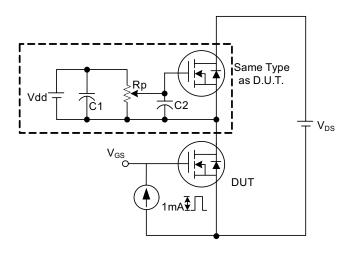


Fig. 3 . 1 Gate Charge Test Circuit

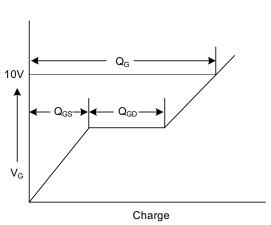


Fig. 3 . 2 Gate Charge Waveform

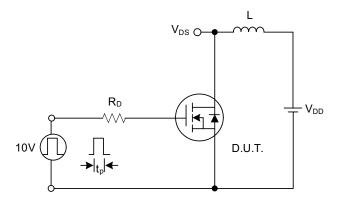


Fig. 4.1 Unclamped Inductive Switching Test Circuit

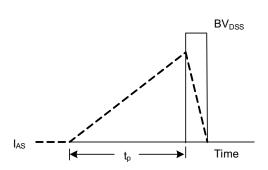


Fig. 4.2 Unclamped Inductive Switching Waveforms



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