



## 40V N-Channel MOSFET

Lead Free Package and Finish

### General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}=1.6\text{ m}\Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

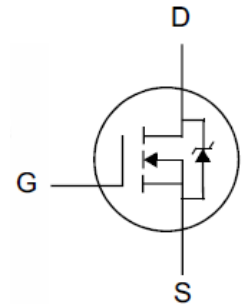
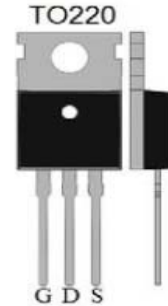
$BV_{DSS}$	$R_{DS(ON),typ.}$	$I_D^{[2]}$
40V	1.6m $\Omega$	280A

### Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- UPS Inverter

### Ordering Information

Part Number	Package	Brand
PTP02N04N	TO-220	



### Absolute Maximum Ratings

$T_C=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	PTP02N04N	Unit
$V_{DSS}$	Drain-to-Source Voltage <sup>[1]</sup>	40	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>[2]</sup>	280	A
	Continuous Drain Current <sup>[3]</sup>	80	
	Continuous Drain Current @ $T_C=100^\circ\text{C}$ <sup>[2]</sup>	210	
$I_{DM}$	Pulsed Drain Current at $V_{GS}=10V$ <sup>[2,4]</sup>	1080	
$E_{AS}$	Single Pulse Avalanche Energy	722	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>[3]</sup>	5.0	V/ns
$P_D$	Power Dissipation	300	W
	Derating Factor above $25^\circ\text{C}$	2.0	W/ $^\circ\text{C}$
$T_L$ $T_{PAK}$	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	$^\circ\text{C}$
$T_J$ & $T_{STG}$	Operating and Storage Temperature Range	-55 to 175	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

### Thermal Characteristics

Symbol	Parameter	PTP02N04N	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	



## Electrical Characteristics

### OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	40	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	5	$\mu A$	$V_{DS}=40V, V_{GS}=0V$
		--	--	100		$V_{DS}=32V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Current	--	--	+100	$nA$	$V_{GS}=+20V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-20V, V_{DS}=0V$

### ON Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	1.6	2.0	$m\Omega$	$V_{GS}=10V, I_D=80A$ [5]
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$

### Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}$	Input Capacitance	--	12.8	--	$nF$	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$
$C_{rSS}$	Reverse Transfer Capacitance	--	0.37	--		
$C_{oss}$	Output Capacitance	--	1.1	--		
$R_G$	Gate Series Resistance	--	3.6	--	$\Omega$	$f=1.0MHz$
$Q_g$	Total Gate Charge	--	129	--	$nC$	$V_{DD}=20V, I_D=100A, V_{GS}=0 \text{ to } 10V$
$Q_{gs}$	Gate-to-Source Charge	--	33	--		
$Q_{gd}$	Gate-to-Drain (Miller) Charge	--	24	--		

### Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	27	--	$nS$	$V_{DD}=20V, I_D=50A, V_{GS}=10V, R_G=10\Omega$
$t_{rise}$	Rise Time	--	85	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	203	--		
$t_{fall}$	Fall Time	--	96	--		

**Source-Drain Body Diode Characteristics** $T_J=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
$I_{SD}$	Continuous Source Current <sup>[2]</sup>	--	--	280	A	Integral PN-diode in MOSFET
$I_{SM}$	Pulsed Source Current <sup>[2]</sup>	--	--	1080		
$V_{SD}$	Diode Forward Voltage	--	0.90	1.2	V	$I_S=80\text{A}$ , $V_{GS}=0\text{V}$
$t_{rr}$	Reverse recovery time	--	55	--	ns	$V_{GS}=0\text{V}$ , $I_F=100\text{A}$ , $di_F/dt=100\text{A}/\mu\text{s}$
$Q_{rr}$	Reverse recovery charge	--	43	--	nC	

**Note:**

- [1]  $T_J=+25^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$  .  
[2] Silicon limited current only.  
[3] Package limited current.  
[4] Repetitive rating; pulse width limited by maximum junction temperature.  
[5] Pulse width $\leq 380\mu\text{s}$ ; duty cycle $\leq 2\%$ .



## Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

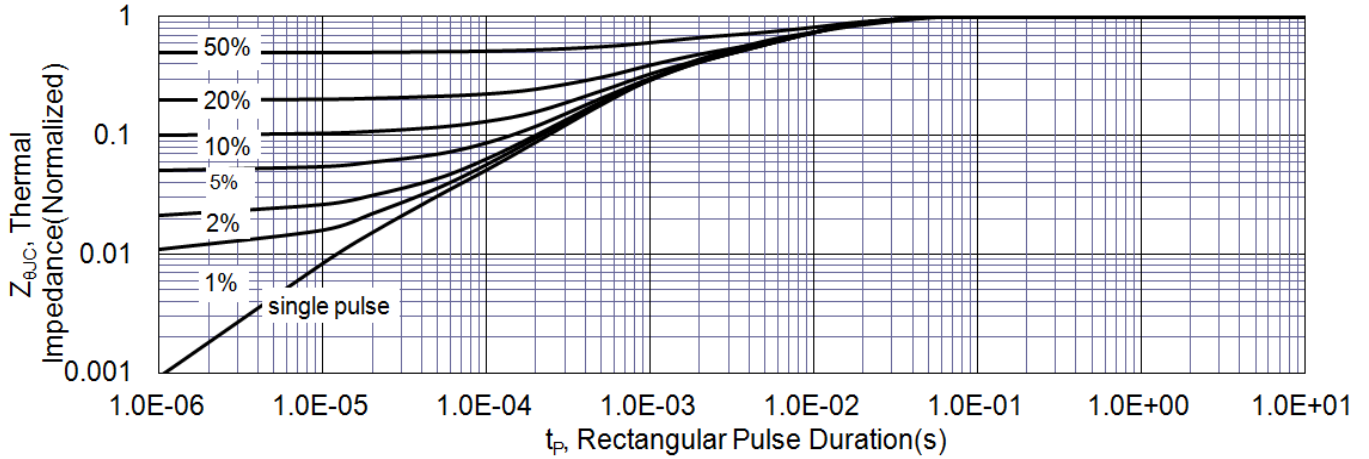


Figure 2. Maximum Power Dissipation vs Case Temperature

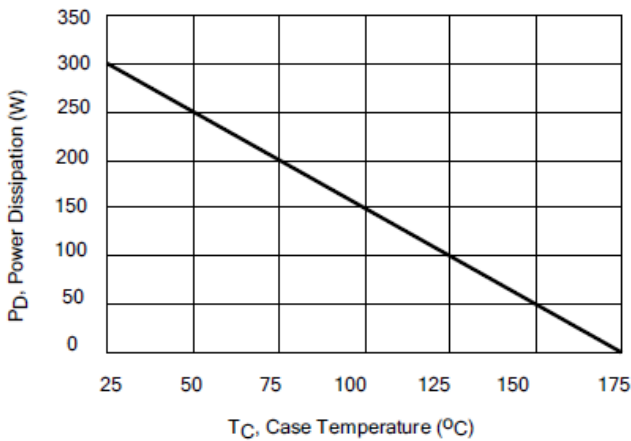


Figure 3. Maximum Continuous Drain Current vs Case Temperature

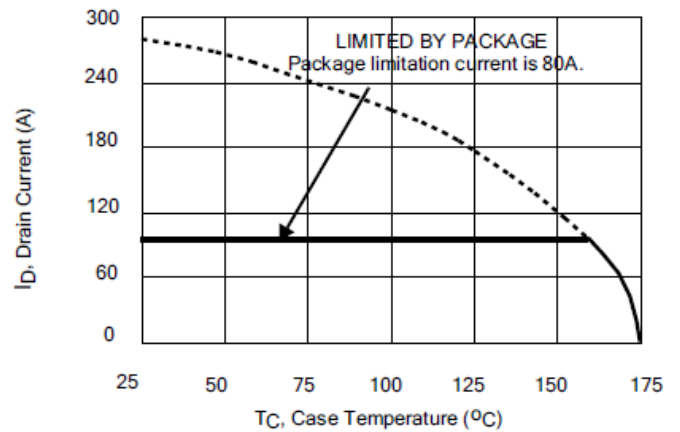


Figure 4. Typical Output Characteristics

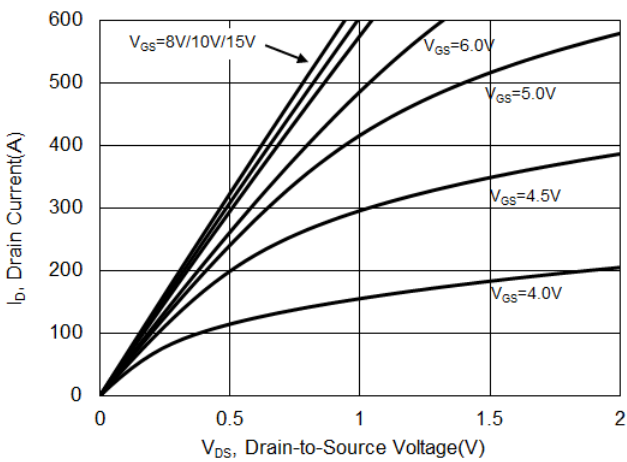
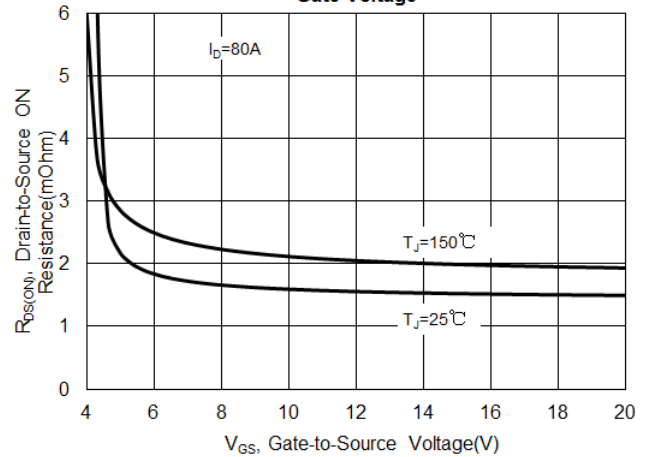


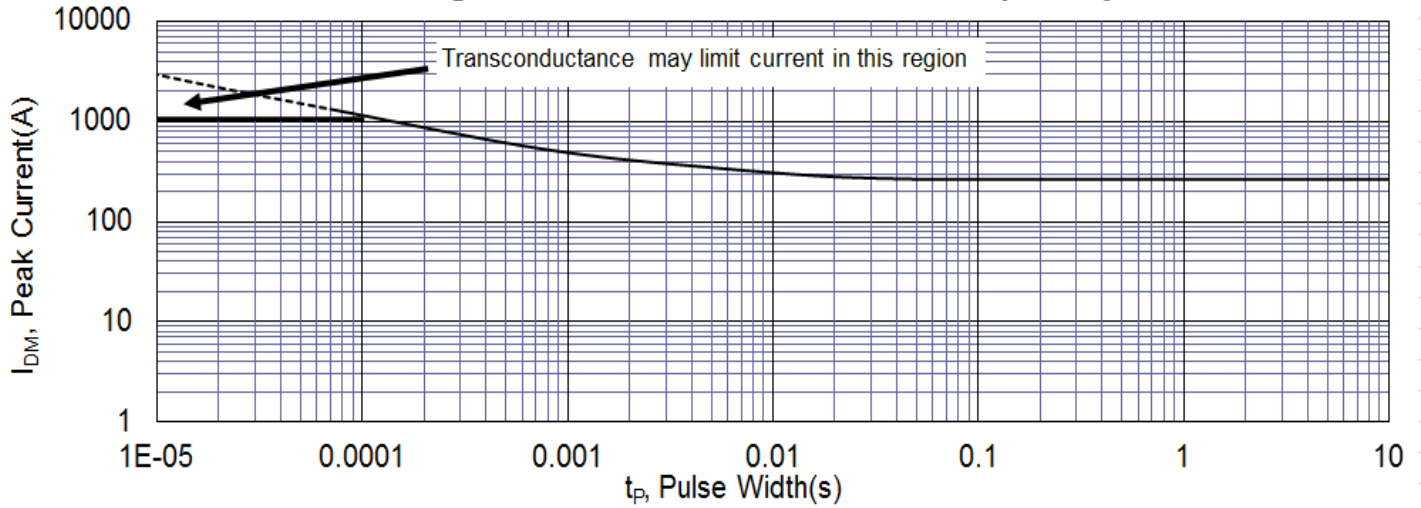
Figure 5. Typical Drain-to-Source ON Resistance vs. Gate Voltage



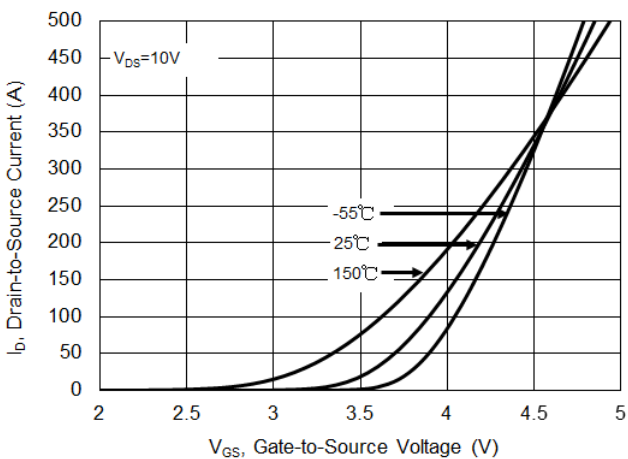


### Typical Characteristics(Cont.)

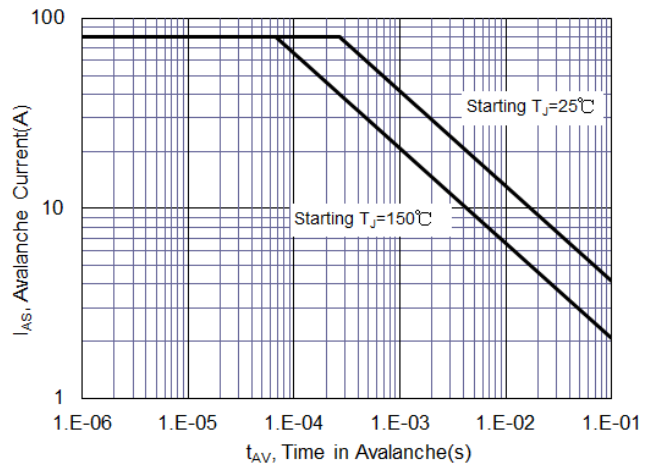
#### Figure 6. Maximum Peak Current Capability



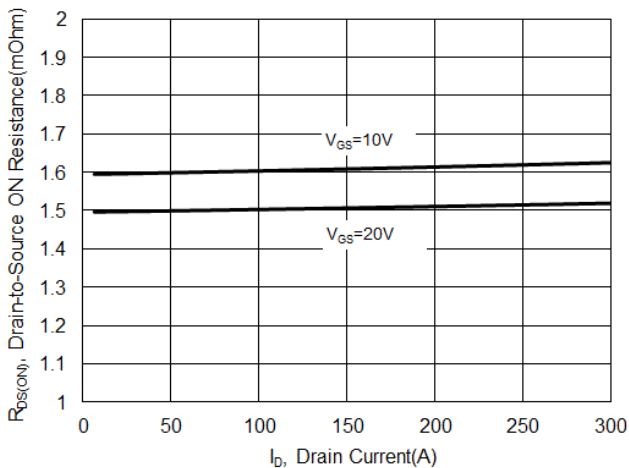
#### Figure 7. Typical Transfer Characteristics



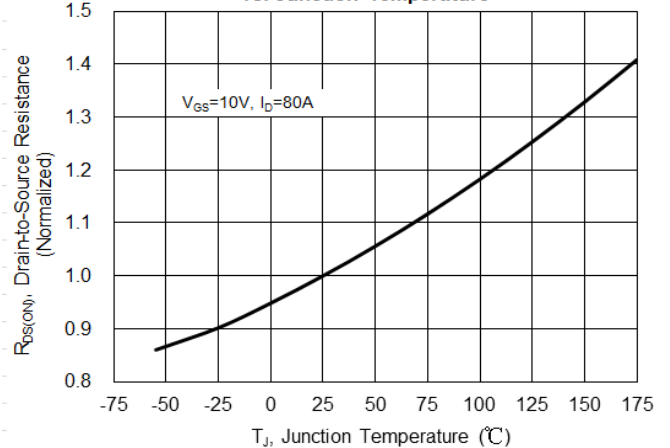
#### Figure 8. Unclamped Inductive Switching Capability



#### Figure 9. Typical Drain-to-Source ON Resistance



#### Figure 10. Typical Drain-to-Source On Resistance vs. Junction Temperature





### Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs. Junction Temperature

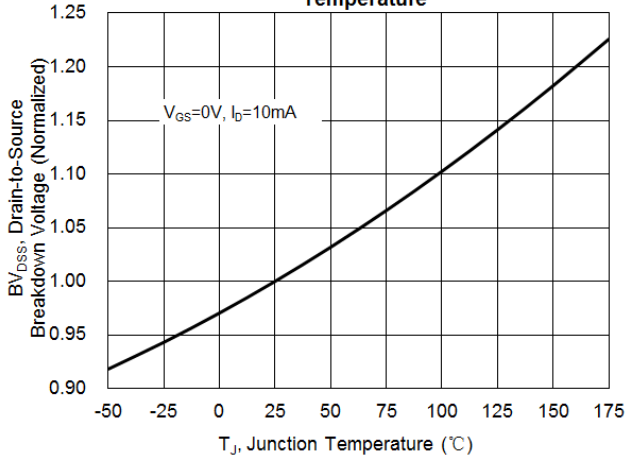


Figure 12. Typical Threshold Voltage vs. Junction Temperature

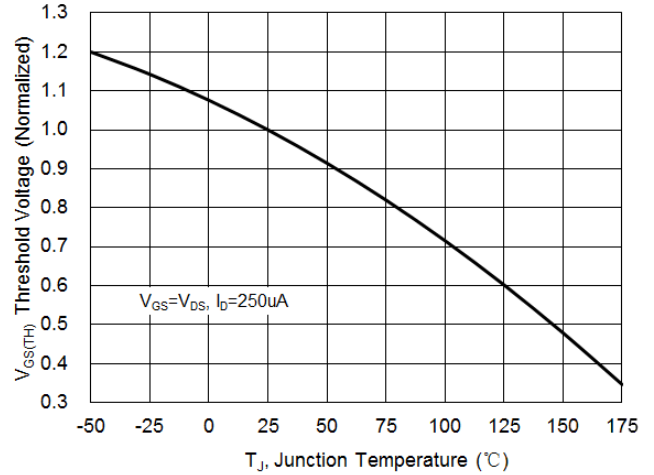


Figure 13. Maximum Forward Safe Operation Area

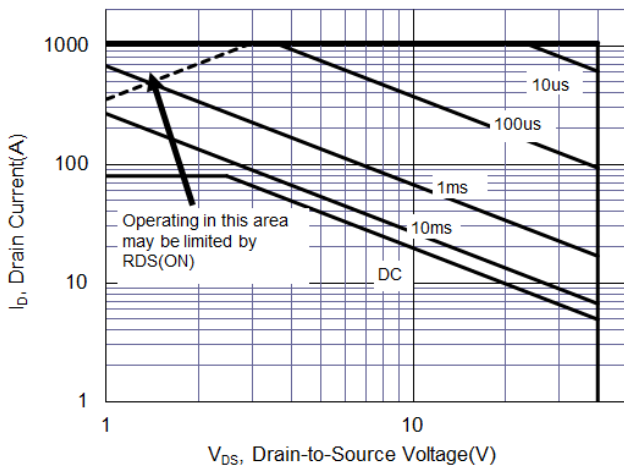


Figure 14. Typical Capacitance vs. Drain-to-Source Voltage

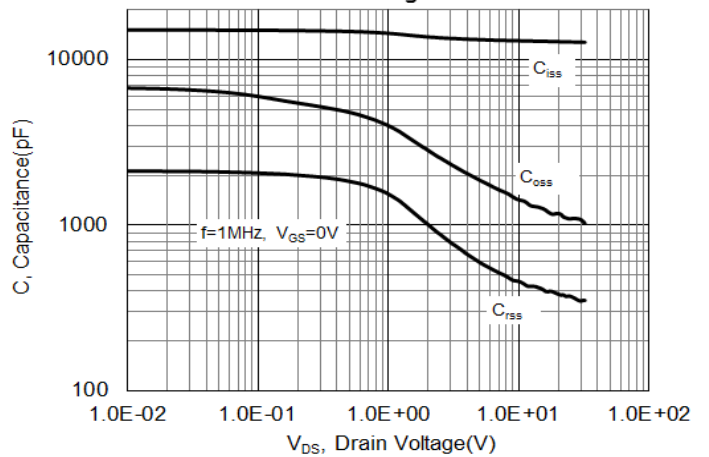


Figure 15. Typical Gate Charge vs. Gate-to-Source Voltage

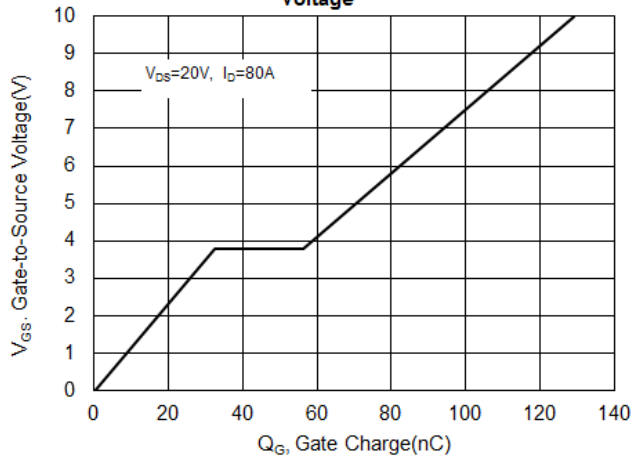
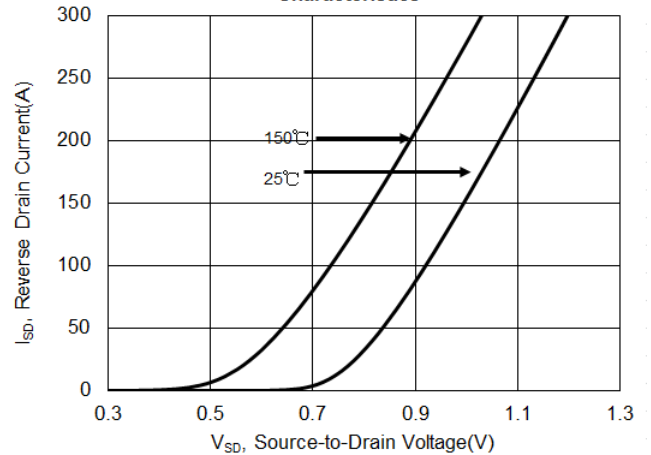


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

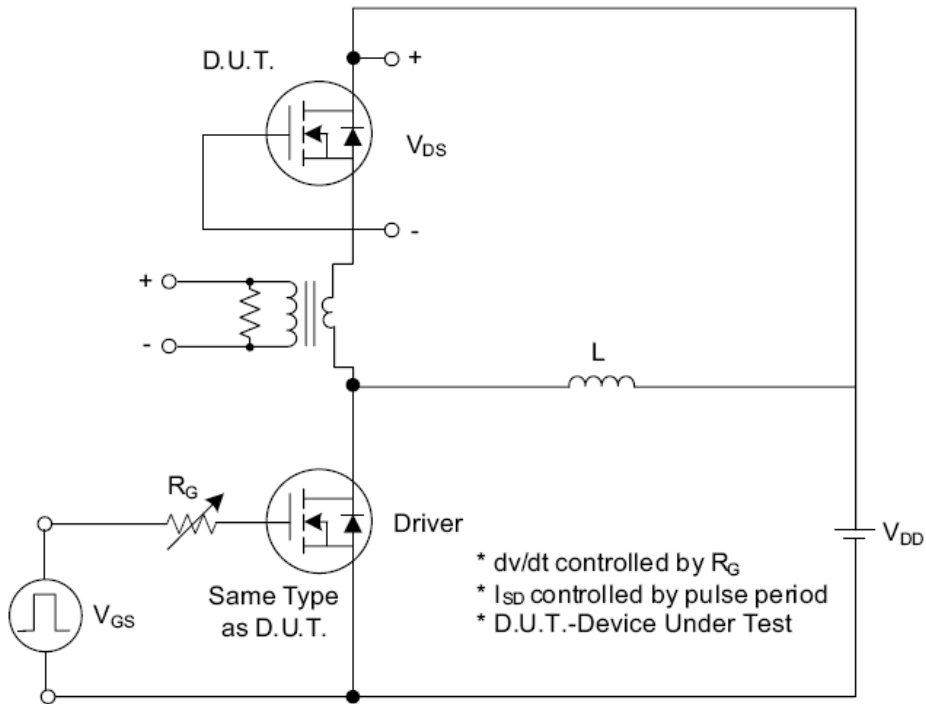


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

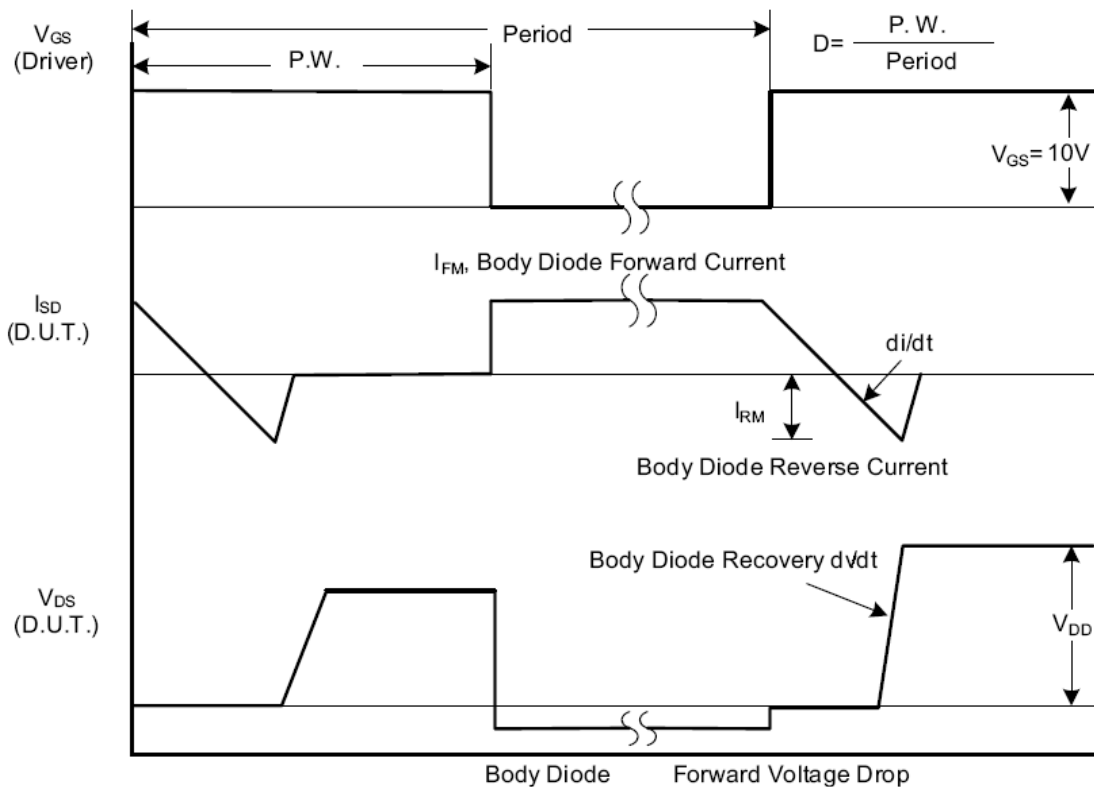


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

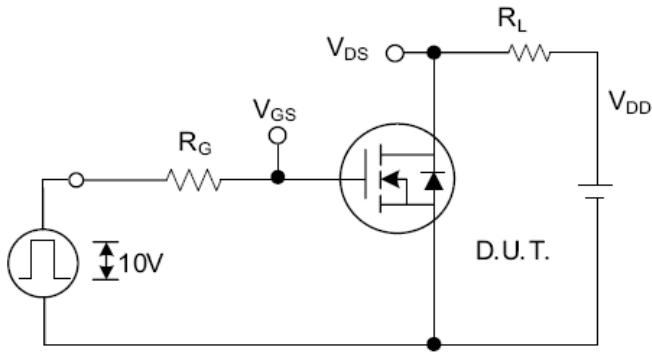
**Test Circuits and Waveforms (Cont.)**


Fig. 2.1 Switching Test Circuit

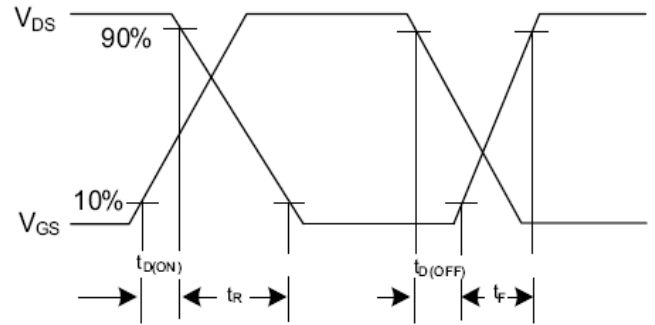


Fig. 2.2 Switching Waveforms

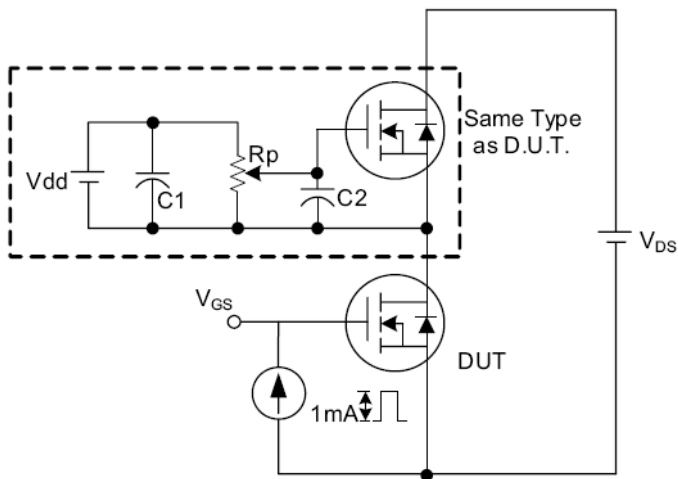


Fig. 3.1 Gate Charge Test Circuit

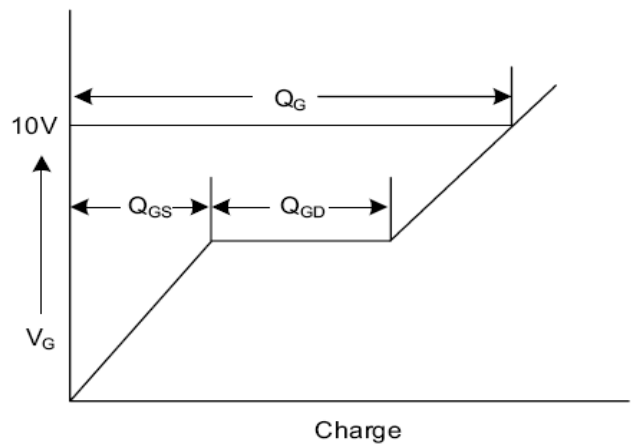


Fig. 3.2 Gate Charge Waveform

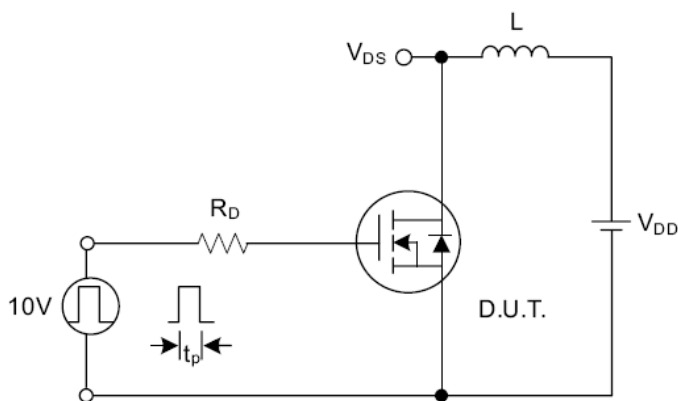


Fig. 4.1 Unclamped Inductive Switching Test Circuit

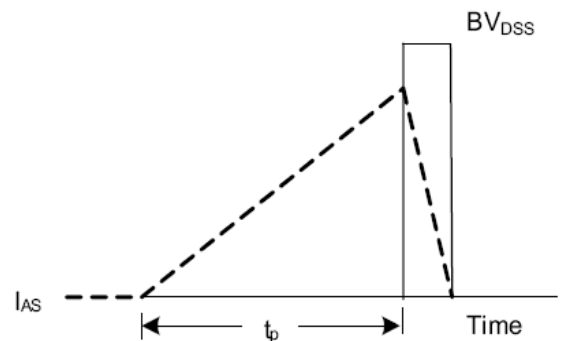


Fig. 4.2 Unclamped Inductive Switching Waveforms





---

## Disclaimers:

Perfect Intelligent Power Semiconductor Co., Ltd (PIP) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to PIP's terms and conditions supplied at the time of order acknowledgement.

Perfect Intelligent Power Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent PIP deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Perfect Intelligent Power Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using PIP's components. To minimize risk, customers must provide adequate design and operating safeguards.

Perfect Intelligent Power Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in PIP's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Perfect Intelligent Power Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of PIP's products with statements different from or beyond the parameters stated by Perfect Intelligent Power Semiconductor Co., Ltd for that product or service voids all express or implied warranties for the associated PIP's product or service and is unfair and deceptive business practice. Perfect Intelligent Power Semiconductor Co., Ltd is not responsible or liable for any such statements.

---

## Life Support Policy:

Perfect Intelligent Power Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Perfect Intelligent Power Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
  - a. are intended for surgical implant into the human body,
  - b. support or sustain life,
  - c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.