

40V N-Channel MOSFET

General Features

- Proprietary New Trench Technology
- ho R_{DS(ON),typ.}=1.65 m Ω @V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- > Fast Recovery Body Diode

Applications

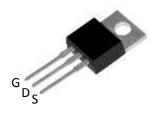
- ➤ High efficiency DC/DC Converters
- > Synchronous Rectification
- UPS Inverter

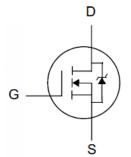
Ordering Information

Dart Number Deckers Brand							
Part Number	Package	Brand					
PTP02N04NB	TO-220	Z					

▶ Lead Free Package and Finish

BV _{DSS}	R _{DS(ON),typ.}	I _D
40V	1.65m Ω	245A





TO-220

Package Not to Scale

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter	PTP02N04NB	Unit
V _{DSS}	Drain-to-Source Voltage ^[1]	40	V
V _{GSS}	Gate-to-Source Voltage	±20	v
	Continuous Drain Current ^[2]	245	
I _D	Continuous Drain Current ^[3]	120	A
	Continuous Drain Current @ Tc=100°C ^[2]	165	
I _{DM}	Pulsed Drain Current at V _{GS} =10V	735	
E _{AS}	Single Pulse Avalanche Energy,L=1mH	1200	mJ
dv/dt	Peak Diode Recovery dv/dt ^[3]	5.0	V/ns
В	Power Dissipation	300	W
P _D	Derating Factor above 25 [°] C	2.0	W/°C
T _L T _{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	°C
T _J & T _{STG}	Operating and Storage Temperature Range	-55 to 175	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTP02N04NB	Unit
$R_{ heta JC}$	Thermal Resistance, Junction-to-Case	0.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	°C/W



Electrical Characteristics

OFF Characteristics T_J =25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40			V	V_{GS} =0V, I_D =250uA
I _{DSS} Drain-to-Source Leakage Curren				1		V _{DS} =40V, V _{GS} =0V
	Drain-to-Source Leakage Current			5	uA	V_{DS} =32V, V_{GS} =0V, T_J =125°C
I _{GSS}	Gate-to-Source Leakage Current			+100	n ^	V _{GS} =+20V, V _{DS} =0V
				-100	nA	V _{GS} =-20V, V _{DS} =0V

ON Characteristics

T_J =25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
R _{DS(ON)}	Static Drain-to-Source On-Resistance		1.65	2.1	mΩ	V _{GS} =10V, I _D =24A
V _{GS(TH)}	Gate Threshold Voltage	2.0		4.0	V	$V_{DS}=V_{GS}$, $I_{D}=250uA$

Dynamic Characteristics

Essentially independent of operating temperature

ynamic Characteristics		Essentially independent of operating temperature				ating temperature
Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
C _{iss}	Input Capacitance		5.1			V 0V
C _{rss}	Reverse Transfer Capacitance		0.37		nF	V_{GS} =0V, V_{DS} =25V, f =1.0MH $_{Z}$
C _{oss}	Output Capacitance		0.91			
Rg	Gate Series Resistance		1.4		Ω	f=1.0MH _Z
Q_g	Total Gate Charge		125			V 20V
Q_{gs}	Gate-to-Source Charge		9.0		nC	V_{DD} =20V, I_{D} =80A, V_{GS} =0 to 10V
Q_{gd}	Gate-to-Drain (Miller) Charge		37			

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
td(ON)	Turn-on Delay Time		10			
trise	Rise Time		24		nS	V_{DD} =20V, I_{D} =24A, V_{GS} = 10V R_{G} =2.5 Ω
td(OFF)	Turn-Off Delay Time		77			
tfall	Fall Time		23			



Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Тур.	Max.	Unit	Test Conditions
I _{SD}	Continuous Source Current			245	۸	Integral PN-diode in
I _{SM}	Pulsed Source Current			735	Α	MOSFET
V _{SD}	Diode Forward Voltage			1.2	V	I _S =24A, V _{GS} =0V
trr	Reverse recovery time		55		ns	V _{GS} =0V ,IF=24A,
Qrr	Reverse recovery charge		35		nC	dir/dt=100A/μs

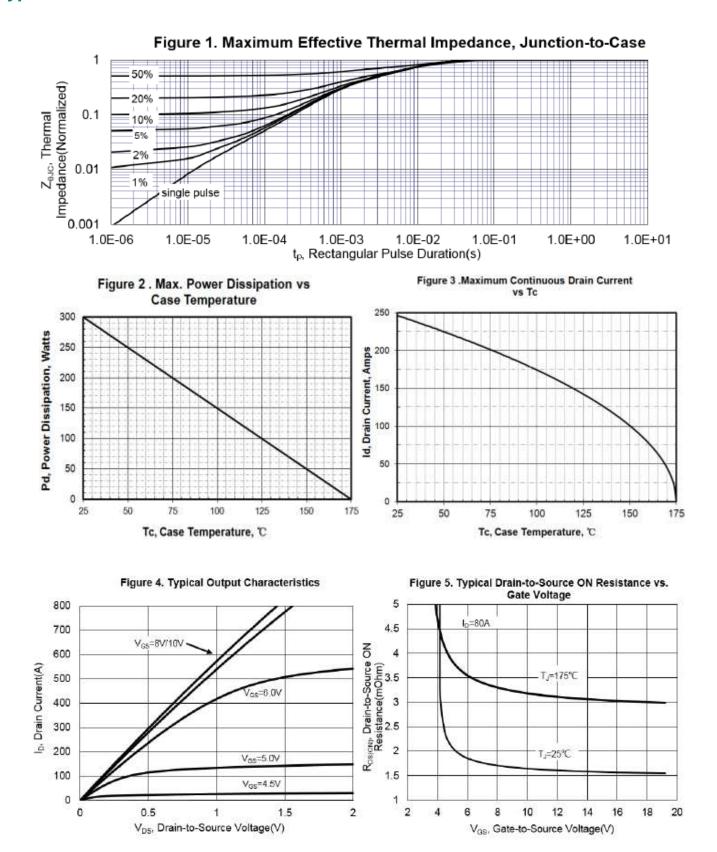
Note:

^[1] T_J =+25°C to +175°C .

^[2] Silicon limited current only.
[3] Package limited current.
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380µs; duty cycle≤2%.

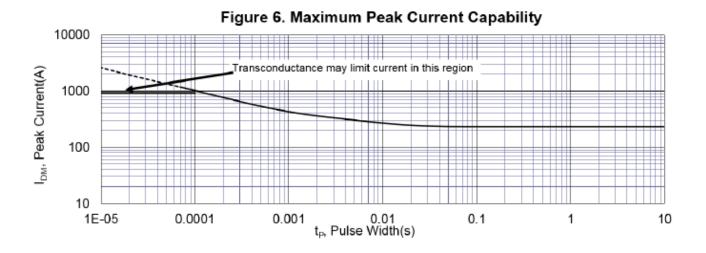


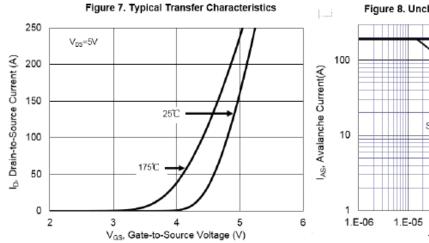
Typical Characteristics

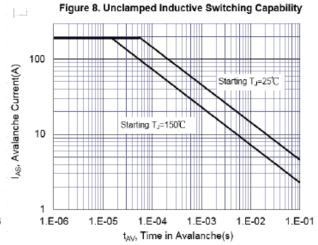


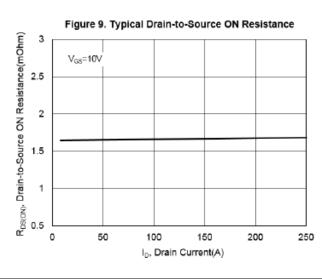


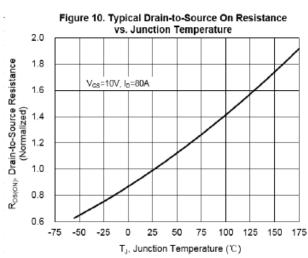
Typical Characteristics(Cont.)





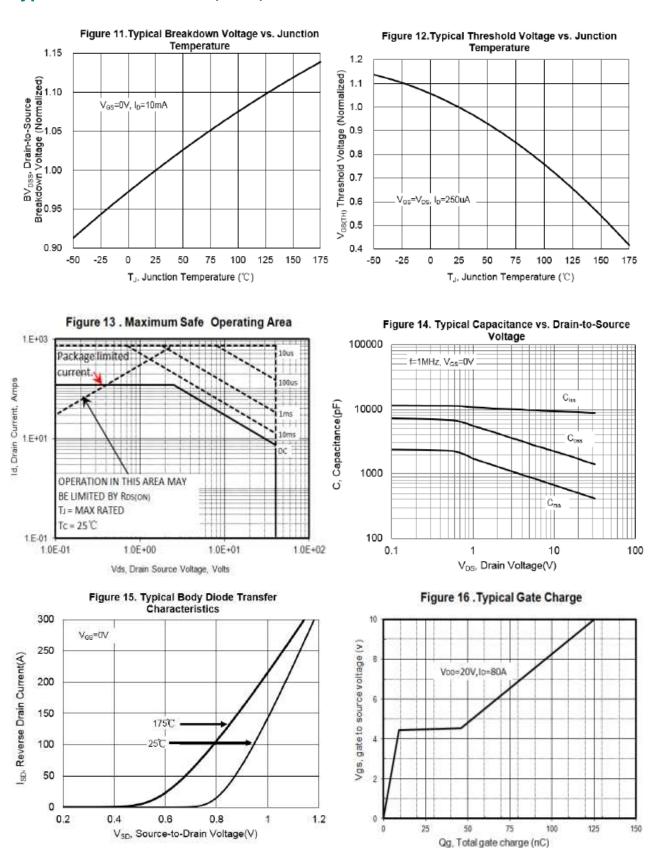








Typical Characteristics(Cont.)





Test Circuits and Waveforms

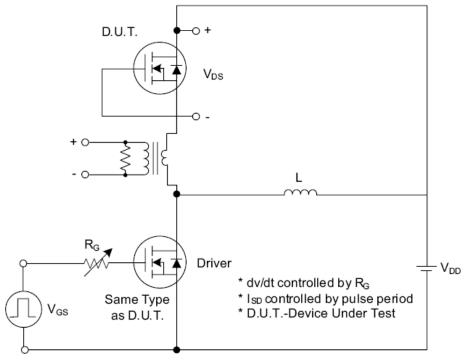


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

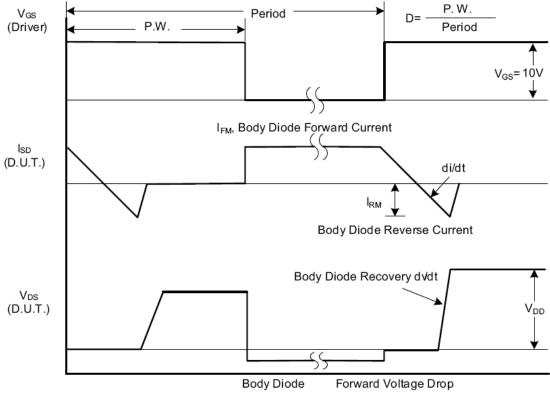


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms (Cont.)

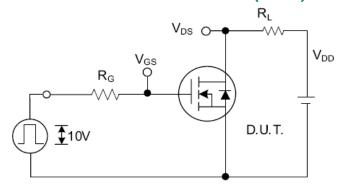


Fig. 2.1 Switching Test Circuit

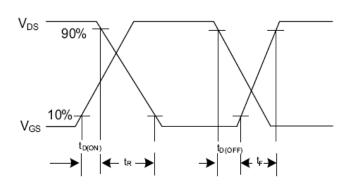


Fig. 2.2 Switching Waveforms

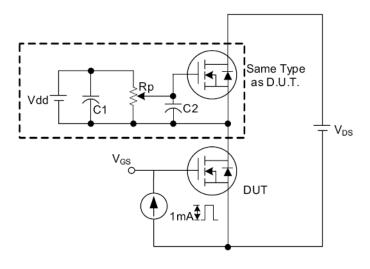


Fig. 3 . 1 Gate Charge Test Circuit

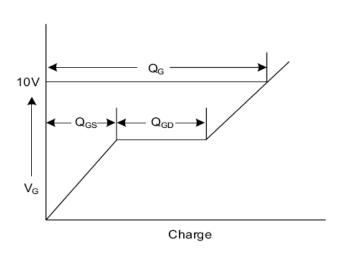


Fig. 3.2 Gate Charge Waveform

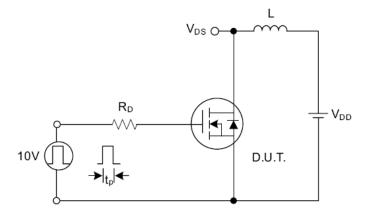


Fig. 4.1 Unclamped Inductive Switching Test Circuit

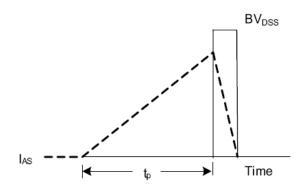


Fig. 4.2 Unclamped Inductive Switching Waveforms



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