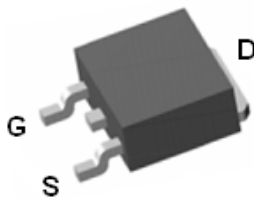


# P6006BD

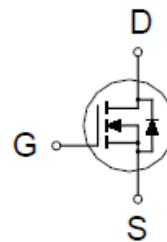
## N-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
60V	60mΩ @ $V_{GS} = 10V$	21A



TO-252



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ °C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	±20	V
Continuous Drain Current	$T_C = 25\text{ °C}$	$I_D$	21	A
	$T_C = 70\text{ °C}$		17	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	85	
Power Dissipation	$T_C = 25\text{ °C}$	$P_D$	50	W
	$T_C = 70\text{ °C}$		32	
Operating Junction & Storage Temperature Range		$T_j, T_{stg}$	-55 to 150	°C

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		75	

<sup>1</sup>Pulse width limited by maximum junction temperature.

# P6006BD

## N-Channel Logic Level Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

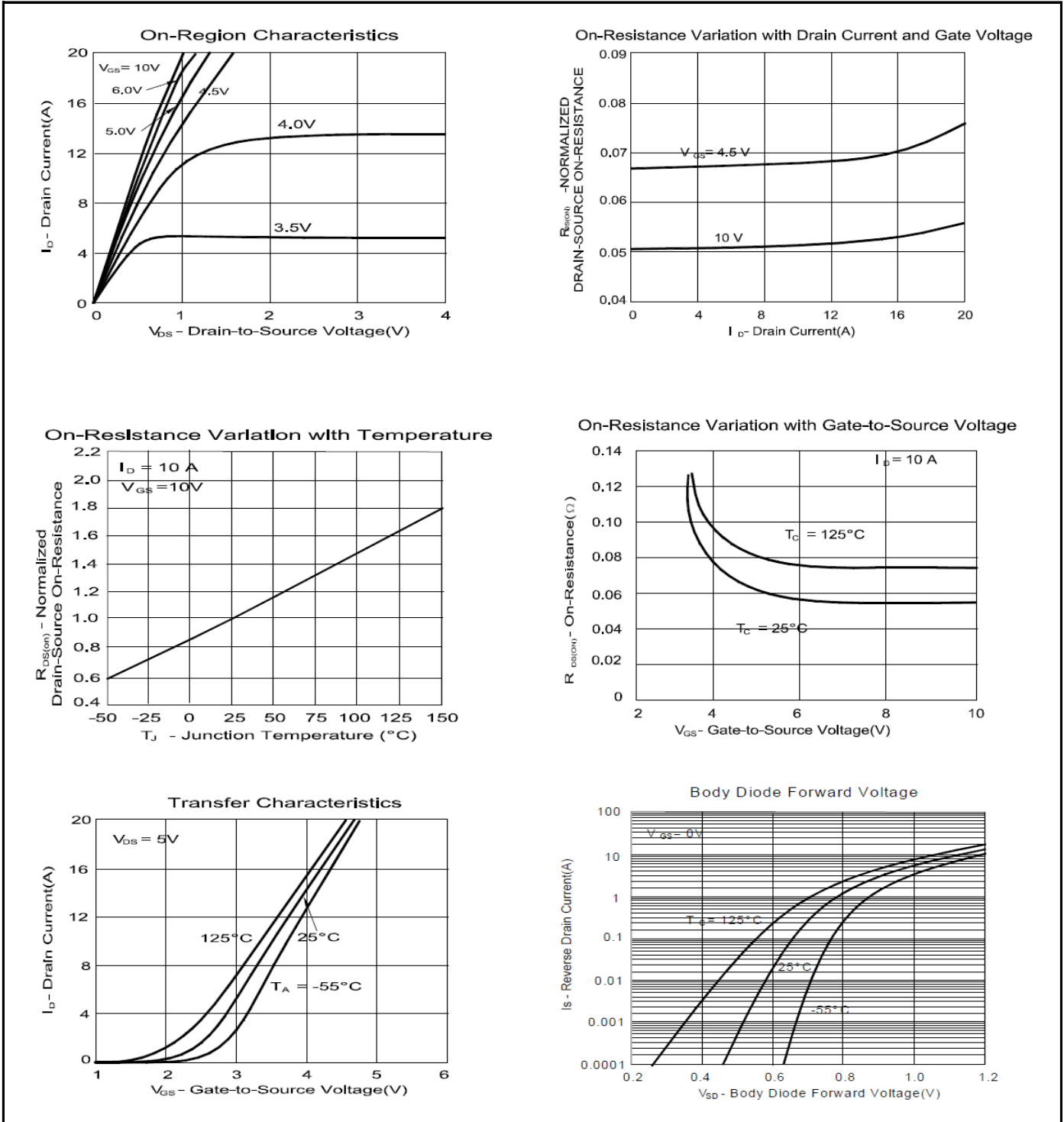
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.5	2.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 10V	21			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 5V, I <sub>D</sub> = 8A		60	80	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A		48	60	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10A		12		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz		584		pF
Output Capacitance	C <sub>oss</sub>			79		
Reverse Transfer Capacitance	C <sub>riss</sub>			44		
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 0.5V <sub>(BR)DSS</sub> , V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		11.5		nC
Gate-Source Charge <sup>2</sup>	Q <sub>gs</sub>			2.1		
Gate-Drain Charge <sup>2</sup>	Q <sub>gd</sub>			2.5		
Turn-On Delay Time <sup>2</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30V, I <sub>D</sub> ≅ 1A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 6Ω		10		nS
Rise Time <sup>2</sup>	t <sub>r</sub>			7.3		
Turn-Off Delay Time <sup>2</sup>	t <sub>d(off)</sub>			17.5		
Fall Time <sup>2</sup>	t <sub>f</sub>			5.5		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>J</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				12	A
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.2	V

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

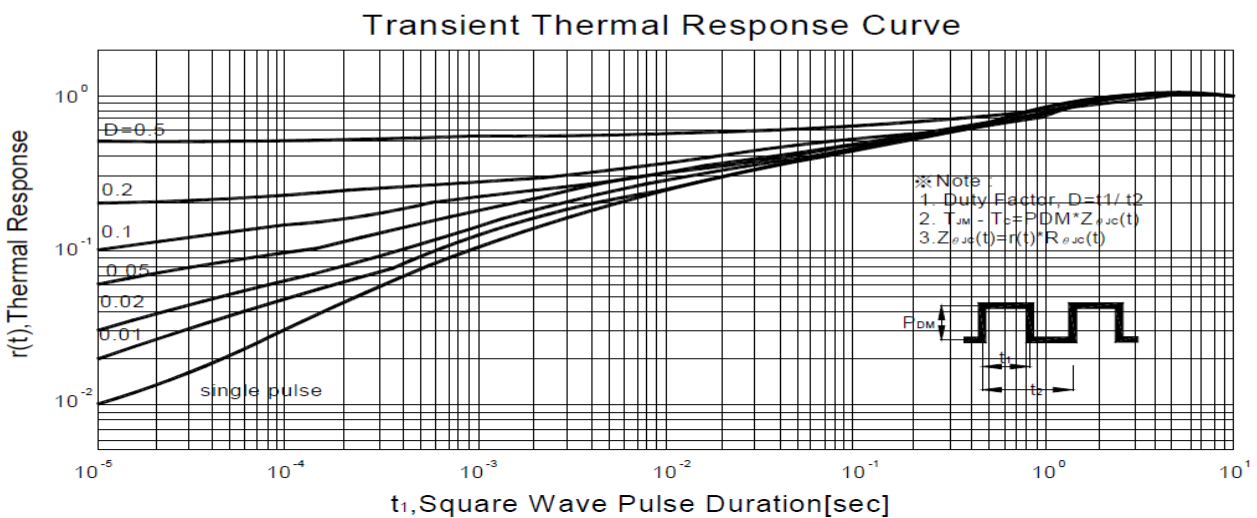
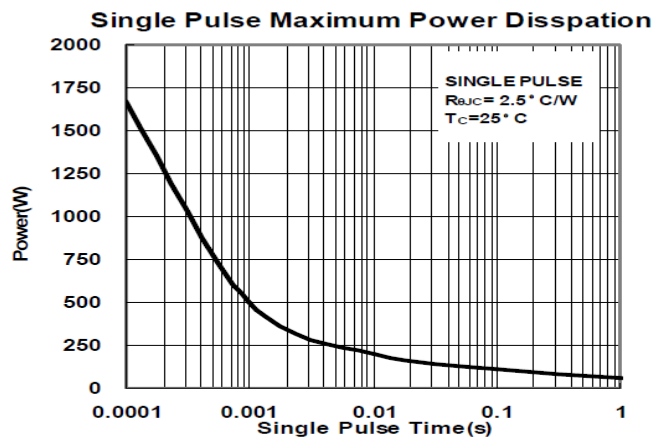
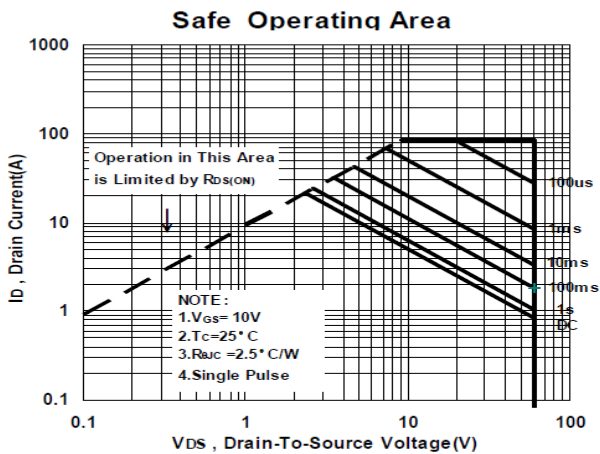
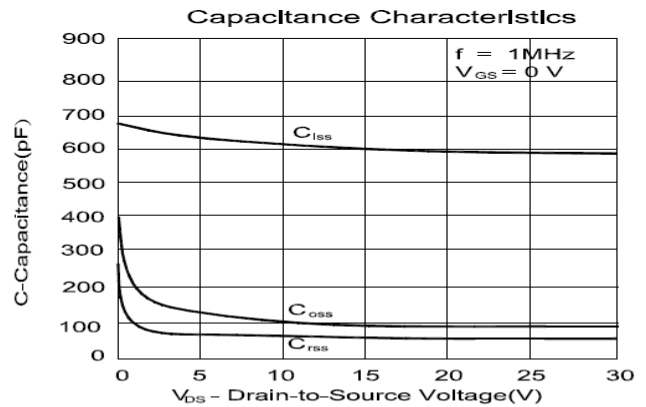
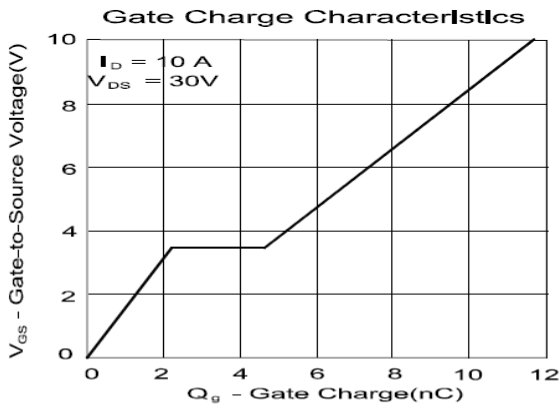
# P6006BD

## N-Channel Logic Level Enhancement Mode MOSFET



# P6006BD

## N-Channel Logic Level Enhancement Mode MOSFET



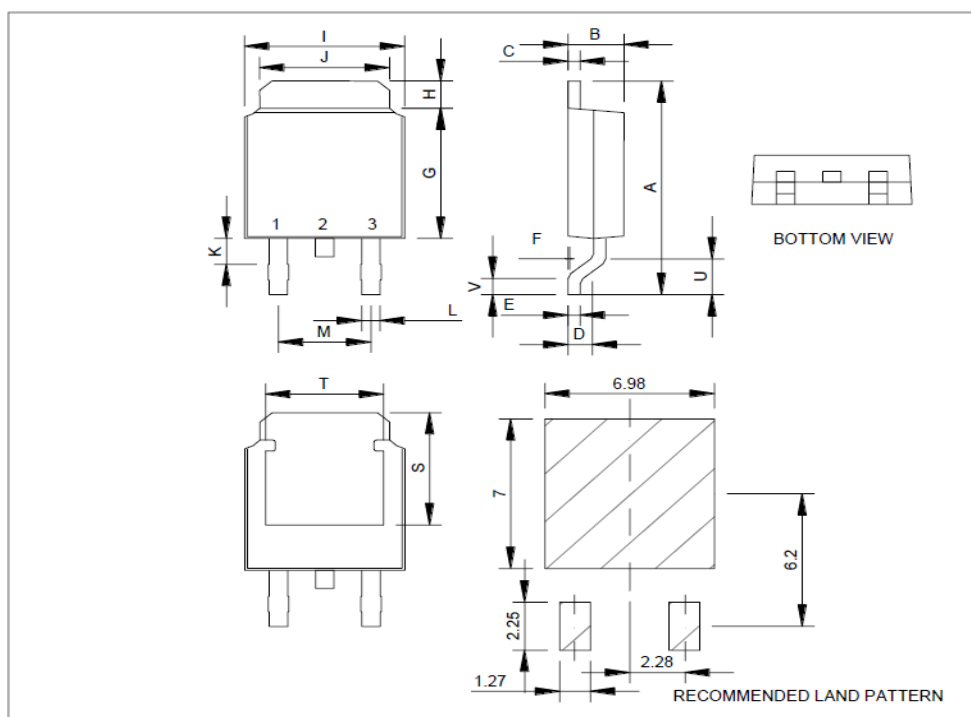
# P6006BD

## N-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

### TO-252 (DPAK) MECHANICAL DATA

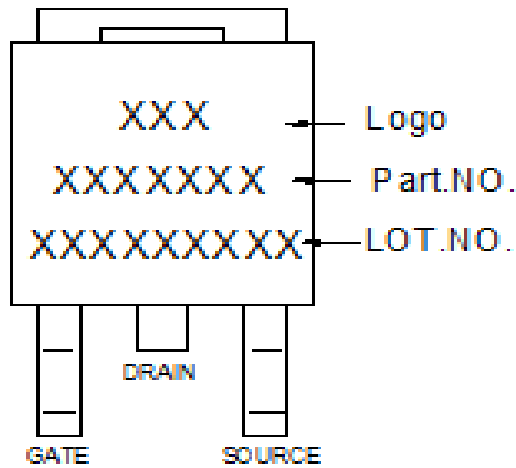
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



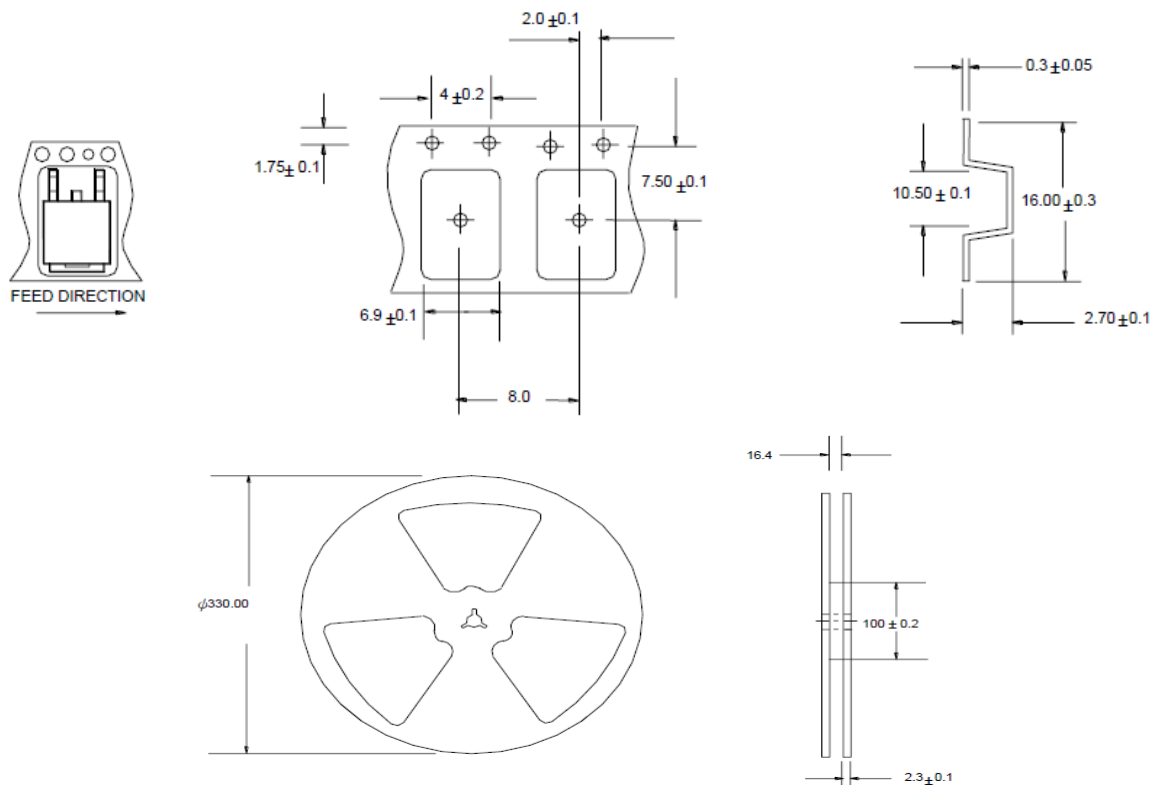
# P6006BD

## N-Channel Logic Level Enhancement Mode MOSFET

### A. Marking Information



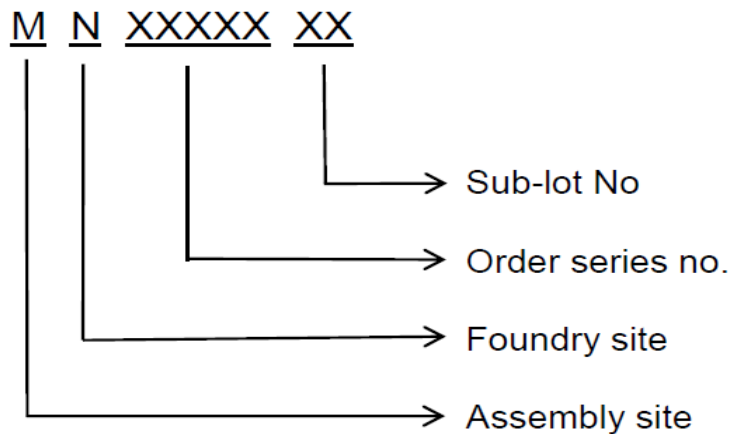
### B. Tape&Reel Information:2500pcs/Reel



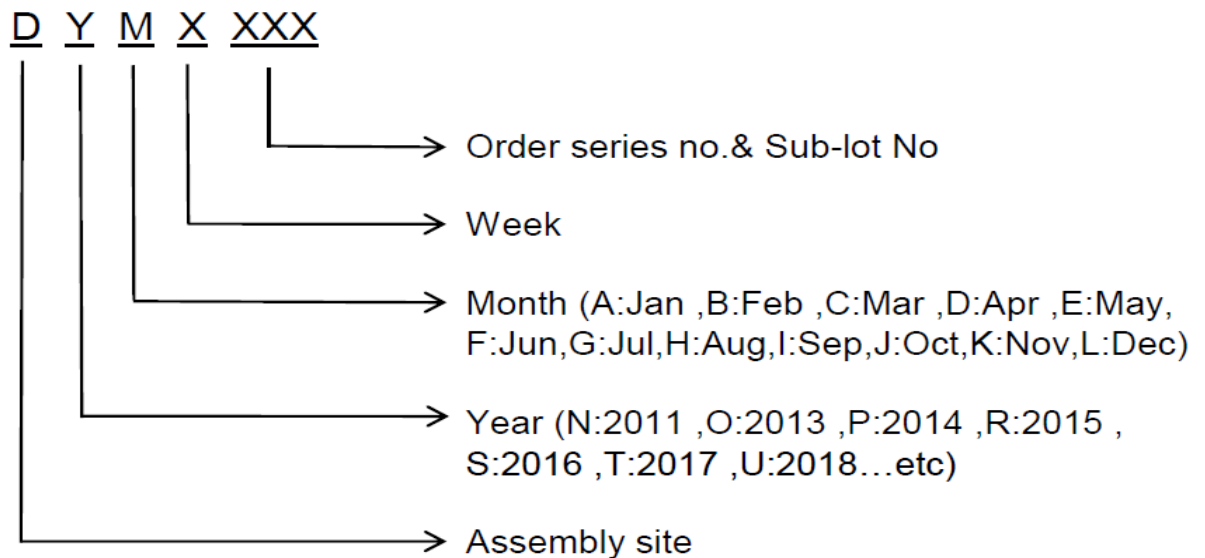
**P6006BD**  
**N-Channel Logic Level Enhancement Mode MOSFET**

**C. Lot No.&Date Code rule**

1.Lot No.



2.Date Code





## P6006BD

### N-Channel Logic Level Enhancement Mode MOSFET

#### D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G"和"Q"的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert "/" between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least